

() 4

MANUFACTURING CONDITION	5021	4791	•••	5021	4791	•••	•••	•••
ING J.	招	L3		H6	[7			
TUR E NC	<u>9</u>	9.		<u>§</u>	<b>양</b>			
MANUFAC	MACHINE NO. H5	MACHINE NO. L3	•••	MACHINE NO. H6	MACHINE NO. L7	•••	•••	•••
MANUFACTURING MANUFACTURING MANUFACTURING TIME AND DATE MACHINE NO. CONDITION	20000101	20000102		20000101	20000102	•••		•••
STEP	STEP A	STEP B	•••	STEP A	STEP B	•••	•••	• •
WAFER		W01			W02		•••	•••
LOT NUMBER	0808-3680							•••
PRODUCT NAME	UPD123							

CO6, 31 ITEM A 20000103 MACHINE NO. T4  : : : : :	C06, 31
TEM B   2000010 	31
: : :	
TEM A 2000010	
TEM B 2000010.	į
•	_
•	
•••	
•••	

WAFER TEST INFORMATION ◆──WAFER CHIP INFORMATION

## FIG. 6A

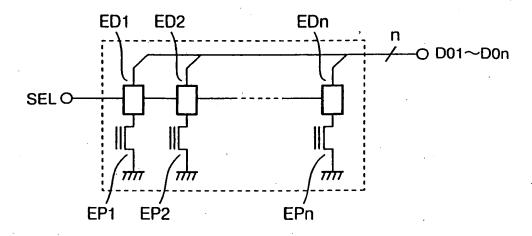
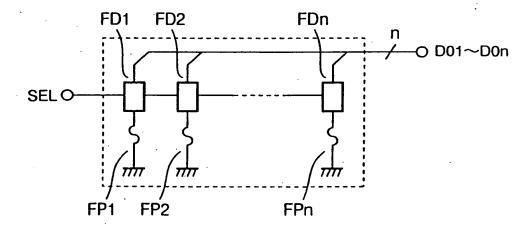


FIG. 6B



#### Title: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES



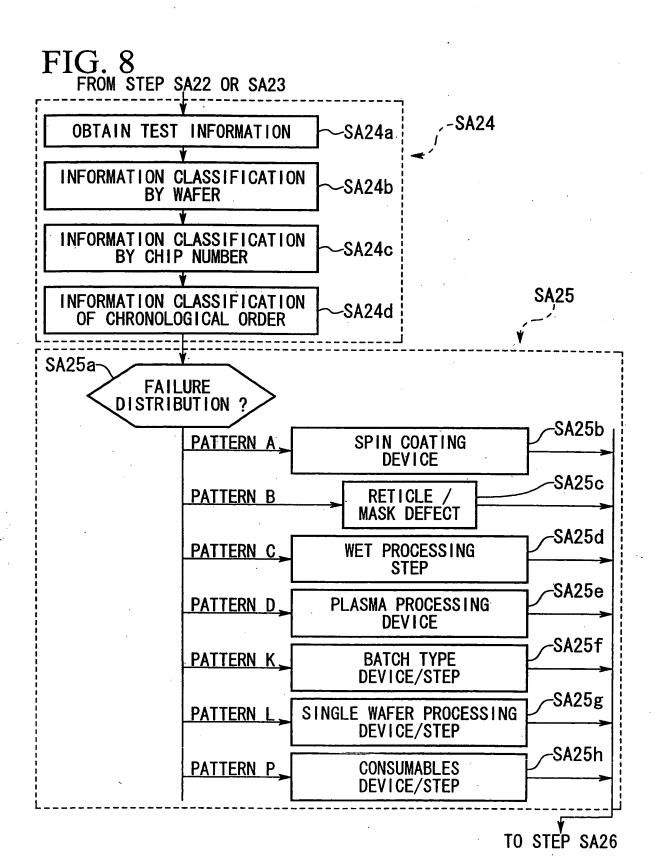
FIG

		-						
JUDGMENT		FAIL			PASS		•••	
	27	FAIL		26	PASS		•••	•••
TEST TEST TEST NAME CONDITION RESULT	7251	5832	•••	7251	5832			•••
	MACH INE NO. H2	MACHINE NO. H2	•••	MACHINE NO. H2	MACHINE NO. H2	<b></b>		•••
TEST TIME AND DATE	20000107 MACHINE NO. H2	TEM 20000107 MACHINE L NO. H2	•••	ITEM 20000107 MACHINE K NO. H2	TEM 20000107 MACHINE L NO. H2	•••	•••	•••
TEST I TEM	I TEM	I TEM		I TEM	LEM		•••	
SAMPLE		000		·	1		•••	• • •
AFER CHIP SAMPLE TEST		co6, 31			1		•••	•••
WAFER			W01					•••
PRODUCT LOT ASSEMBLY WA NUMBER LOT NUMBER NUMBER			UPD123 -3030 35ER-008	533				•••
LOT NUMBER		CB95	-3030					•••
PRODUCT NAME			UPD123					•••

ASSEMBLY TEST INFORMATION ASSEMBLY CHIP INFORMATION

#### Title: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES

Inventor(s): Sumio OGAWA et al. Docket No.: 088941-0203



Docket No.: 088941-0203

# FIG. 9

	FAILURE DISTRIBUTION PATTERN	FAILURE CAUSE	IMPROVEMENT AREA
A		WHEN PROCESSING SOLVENT IS COATED ON ROTATING WAFER, LIQUID LEFT IN NOZZLE DRIPS AND MAKES FILM THICKNESS INCONSISTENT, AND HENCE CONTACT FAILURE OCCURS.	·RESIST COATING DEVICE ·SOG FILM DEPOSITING DEVICE
В		WHEN A PLURALITY OF CHIPS IS EXPOSED AT THE SAME TIME IN RETICLE, IF A PART OF RETICLE IS DEFECTIVE, FAILURES OCCUR AT A SPECIFIC LOCATION IN EACH EXPOSURE.	RETICLE
С		WHEN VERTICALLY MOUNTED WAFER IS IMMERSED IN PROCESSING LIQUID, DIFFERENCE IN PROCESSING TIME OCCURS BETWEEN UPPER AND LOWER PART OF THE WAFER, AND HENCE FAILURES OCCUR CONCENTRATED IN THE UPPER PART OR LOWER PART.	•WET ETCHING DEVICE /STEP •BATCH TYPE CLEANING DEVICE /STEP
D		IN THE PLASMA ETCHING DEVICE, ELECTRIC FIELD BECOMES INCONSISTENT IN THE PERIPHERY OF THE WAFER, AND HENCE FAILURES OCCUR IN THE PERIPHERY OF THE WAFER.	-PLASMA PROCESSING DEVICE
	:	:	•

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#### **FIG.10**

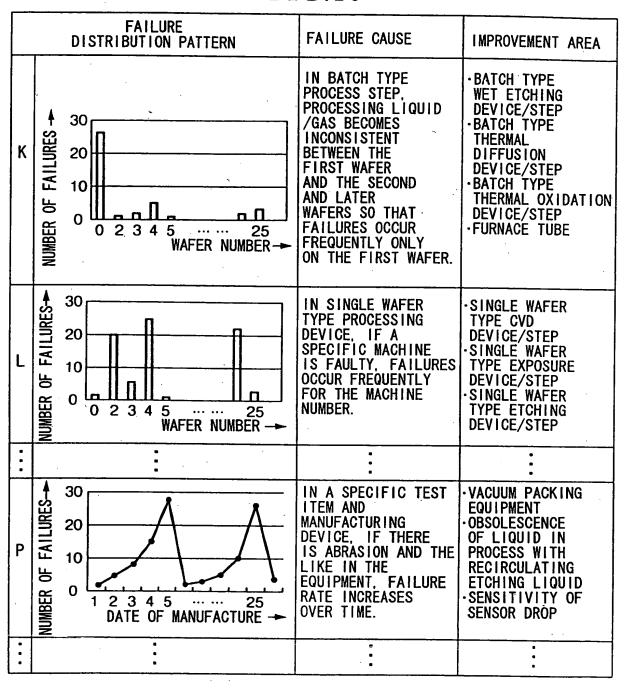


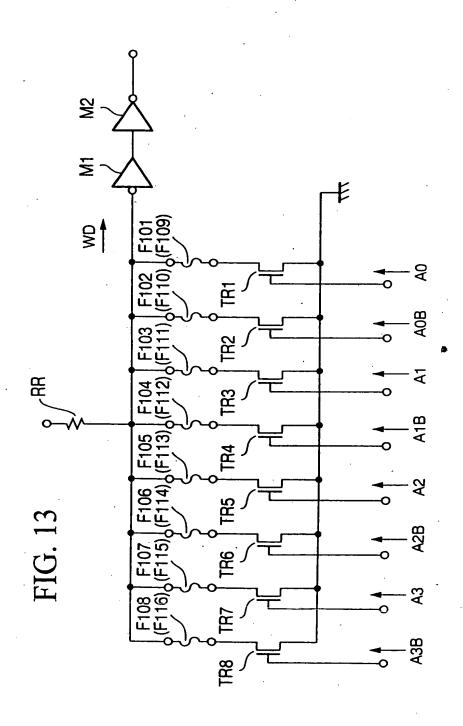
FIG. 11 100-MANUFACTURING INCOMING HISTORY 20 WAFER INFORMATION WAFER WAFER TEST MANUFACTURING LINE 23 INFORMATION (INCLUDE CHIP INFORMATION) LSI TESTER DEFECTIVE 24a-FAIL **CELL TEST** - SCRAP INFORMATION (INCLUDE CHIP **PASS** REPLACEMENT INFORMATION) **ADDRESS** TRIMMING DEVICE DECISION DEVICE WAFER TESTER 22-24b FAIL - SCRAP **PASS** 26 **PACKAGE** ASSEMBLING DEVICE -28 **ASSEMBLY** -27 **TEST ASSEMBLY TESTER** INFORMATION 29-**FAULT PRODUCTS** NON-REPLACEMENT ADDRESS DEFECTIVE **PRODUCTS** 42 READING DEVICE -33 CHIP POSITION SHIPPING ANALYZING DEVICE FAILURE DISTRIBUTION MAPPING DEVICE 32 FAILURE CAUSE DETERMINING DEVICE

35

34

$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	R3 ; WAFER NO. ("WXX01")   ; ; VREF FUSE NO. (FY101")   ; VREF FUSE NO. (FY102")   ;	R6 ; CHIP NO. ("CA001")   ; ;ROW FUSE NO. ("FB101")   ;ROW FUSE NO. ("FB102")   ;	$R9 \sim \{ ; col FUSE NO. ("FC101") \} \{ ; col FUSE NO. ("FC102") \} \dots R7$	R11 ; CHIP NO. ("CA002") ; ;ROW FUSE NO. ("FB201") ; ;ROW FUSE NO. ("FB202") ];	R14{ ; COL FUSE NO. ("FC201") ]; [ ; COL FUSE NO. ("FC202") ]; R13	: TERMINATION DELIMITER OF WAFER INFORMATION ("/E")   1. R18	R17~~\:WAFER NO. ("WXXO2")];	R20 ; CHIP NO. ("CB101")   ;   ; ROW FUSE NO. ("FD101")   ; ROW FUSE NO. ("FD102")   ;	$R23 \sim \{ : COL FUSE NO. ("FE101") ]; \cdots [ : COL FUSE NO. ("FE102") ]; \cdots R21 R22 R22$		R25
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### FIG. 14

[ L	ROW	FUSE	FIRST	NO.	("F101".	GR1)	R51
۲,	ROW	FUSE	FIRST	NO.	("F109".	GR2)	R52
┗.				•			
<u>.</u>				•			7
Ĺ.	COL	FUSE	FIRST	NO.	("F501".	GL1)	R61
L	COL	FUSE	FIRST	NO.	("F509".	GL2)	R62

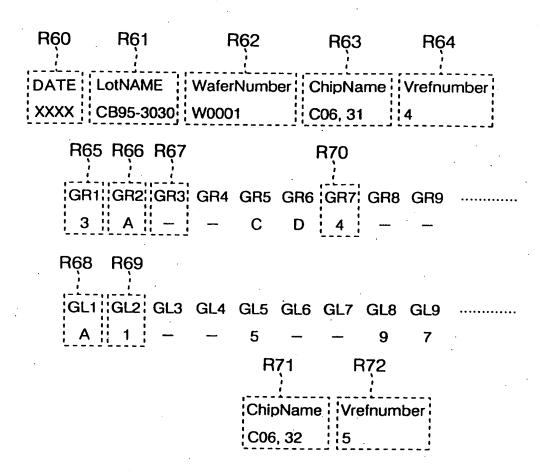
#### FIG. 15

```
PRODUCT NAME
LOT NAME ("LOT NO".
                      CB95-3030)
WAFER NO. ("W0001")
VREF FUSE NO.
                ("FY101")
VREF FUSE NO.
                ("FY102")
CHIP NO.
          ("CA001")
ROW FUSE NO.
               ("F101")
ROW FUSE NO.
ROW FUSE NO.
ROW FUSE NO.
               ("F108")
ROW FUSE NO.
ROW FUSE NO.
ROW FUSE NO.
ROW FUSE NO.
COL FUSE NO.
               ("F501")
COL FUSE NO.
               ("F503"
COL FUSE NO.
               ("F514")
COL FUSE NO.
               ("F516")
```

TERMINATION DELIMITER OF WAFER INFORMATION ("/E")

- 1

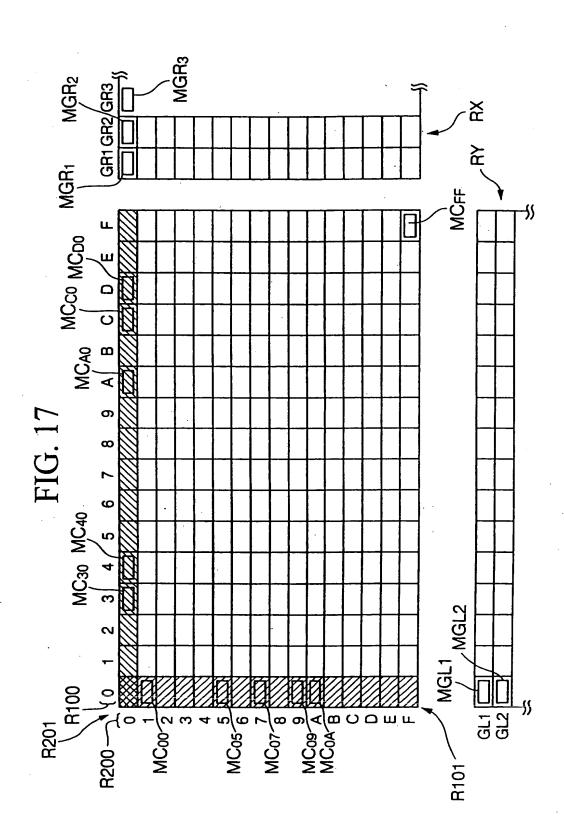
### FIG. 16

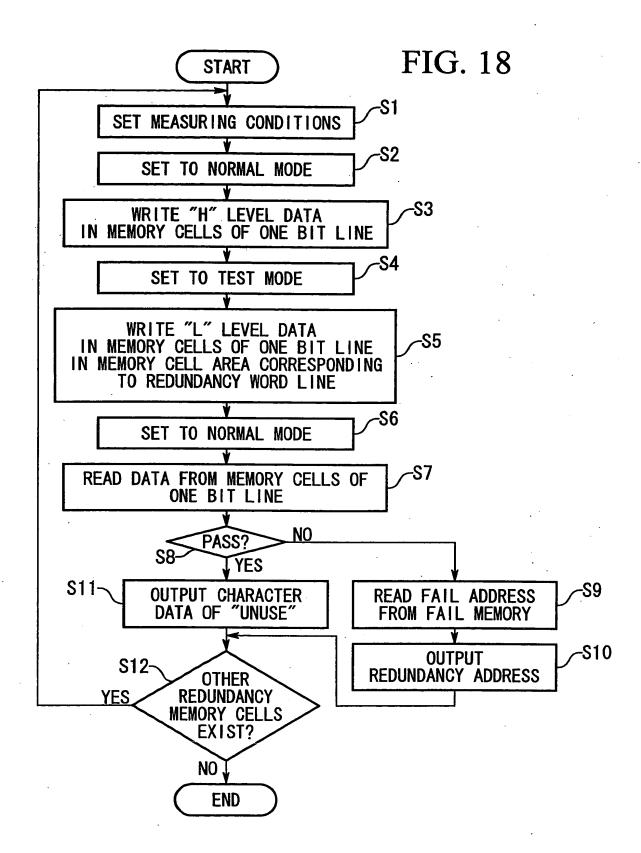


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## FIG. 19

#### X-Redundancy RoLL C

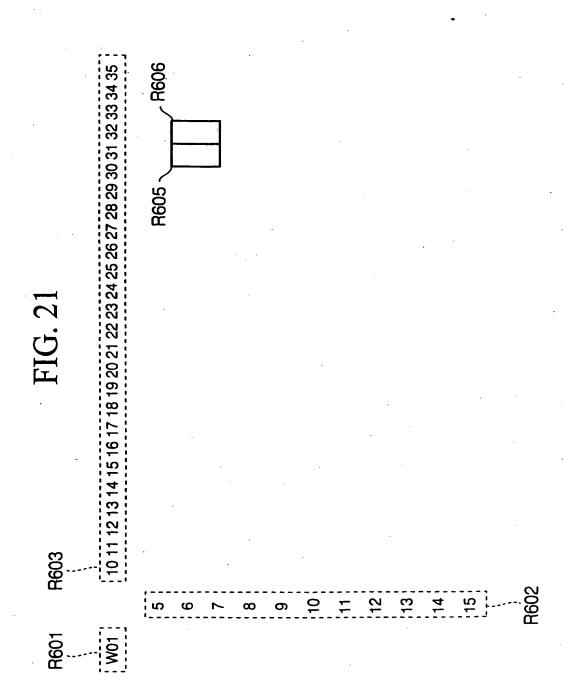
FUSE	REDUNDANCY	ADDRESS
F101 ~F108	3	R301
F109~F116	Α	R302
F117~F124	UNUSE	R303

#### Y-Redundancy RoLL C

FUSE	REDUNDANCY ADDRESS
F501 ~F508	A R351
F509 ~F516	1
F517 ~F524	UNUSE

# FIG. 20

R4(	)1 R4(	02 R4	03 R4	04 R5	05
	WAFER STEP LOT NO	ASSEMBLY LOT NO	WAFER NO	CHIP NO	SAMPLE NO
·	CB95-3030	35er008	`[W01]	C06, 31	`UII
	CB95-3030	35er008	W01	C06, 32	2
	•	•	•	•	•



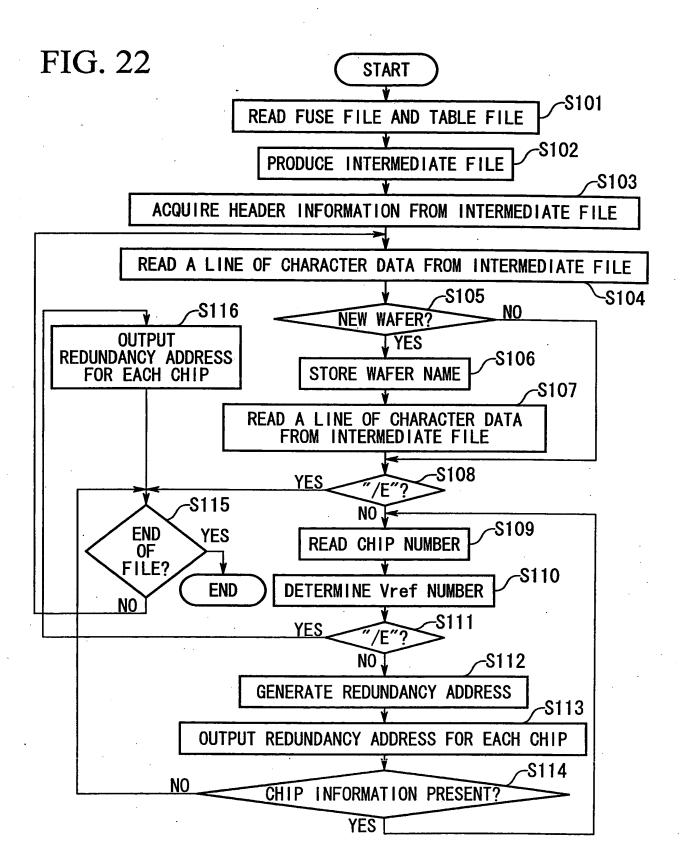


FIG. 23

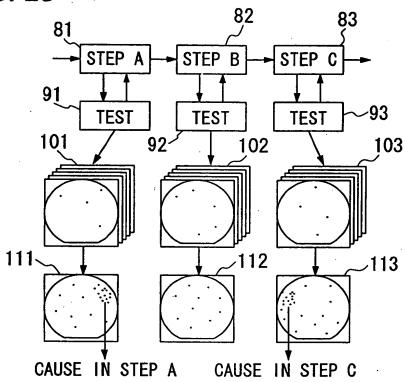
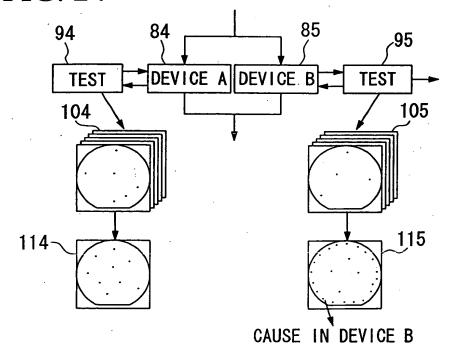


FIG. 24



# Title: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICES

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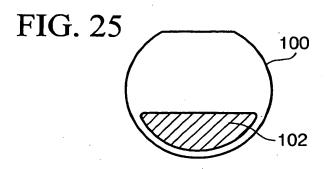


FIG. 26

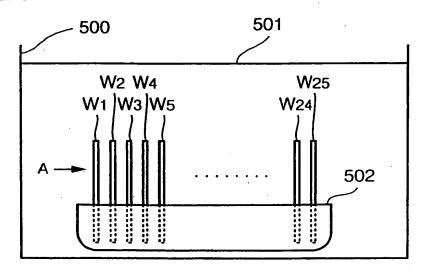


FIG. 27

